PRODUCT RELIABILITY REPORT

Platform: INN040FQ045A-Q

--40V E-Mode GaN FET

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1. Platform Information

Platform	Automotive S40E2.0A
Product	INN040FQ045A-Q
Package	FCQFN (3mm x4mm)
BV Rating(V)	40
Process Technology	GaN on Silicon

2. Scope

This reliability Qual. report is summarized the results of INN040FQ045A-Q product, which followed by AEC-Q101-Rev-E standard*.

3. Pass/Fail criteria

3.1 Pre- and Post- stress test electric parameters

All pre- and post-stress parts must be tested the static electrical parameters defined in the datasheet at room temperature. The criteria as below:

Parameter	Datasheet specification	Criteria: Pre- and post-parameter shift or ratio	Test Item
Vth	Min: 0.7V Max: 2.4V	Within 20%	All reliability tests followed
Rdson	Max: 4.5mΩ	Within 20%	All reliability tests followed
Igss(-)	Max: 20uA	Within 5X	Except moisture related tests, other tests followed
		Within 10X	Moisture related tests followed
Igss(+)	Max: 80uA	Within 5X	Except moisture related tests, other tests followed
		Within 10X	Moisture related tests followed
Idss	Max: 200uA	Within 5X	Except moisture related tests, other tests followed
		Within 10X	Moisture related tests followed

***Note:** All electrical parameter test at Innoscience's reliability Lab, and the Lab environment conditions as below:
Temperature: 25±5°C
Humidity: (30~70) % RH

3.2 Other item criteria

Item	Pass/Fail criteria
Solderability	The inspected area of each lead must have 95% solder coverage minimum;
TCDT	Follow customer standard: random choose 5pcs sample to check DPA, analysis the point with highest stress and related gate, source, drain three points.
DPA	Check no corrosion, contamination, delamination and metal hole and the crack or defect between device and substrate;

4. Reliability Tests

Innoscience's E-mode GaN FET was subjected to a variety of reliability tests under the conditions referenced to AEC-Q101 standard. These test items and results were shown as below:

NO.	Test Items	Test Condition	Sample Size Unit *lot	#Fail	Result
1	HTRB	Ta=150°C, Vd=40V, VG=VS=0V, 1000hrs	77*3	0 Fail	Pass
2	HTGB(+)	Ta=150°C, VG=6V, VD=VS=0V, 1000hrs	77*3	0 Fail	Pass
3	HTGB(-)	Ta=150°C, VG=-4V, VD=VS=0V, 1000hrs	77*3	0 Fail	Pass
4	LTRB	Ta=-40°C, VD=40V, VG=VS=0V, 1000hrs	77*3	0 Fail	Pass
5	LTGB(+)	Ta=-40°C, VG=6V, VD=VS=0V, 1000hrs	77*3	0 Fail	Pass
6	ESD-HBM	Ta=25°C	30*1	0 Fail	±500V
7	ESD-CDM	Ta=25°C	30*1	0 Fail	±500V
8	MSL1	T=85°C, RH=85% , 3 x reflow, 168hrs	25*3	0 Fail	Pass
9	H3TRB	Ta=85°C, 85%RH, Vd=32V, 1000hrs	77*3	0 Fail	Pass
10	TC	-55°C /+150°C, 15°C /min, 5mins dwell time, 1000cycles	77*3	0 Fail	Pass
11	TCDT	Random 2parts after TC, analysis the highest stress point and related gate, drain, source points	2*3	0 Fail	Pass
12	uHAST	Ta=130°C, 85%RH, 96hrs	77*3	0 Fail	Pass
13	TS	Ta=-55°C to 150°C, Transfer time:10s, 15mins dwell time, 1000cycles	77*3	0 Fail	Pass
14	IOL	ΔTj =125°C, ton/ toff=1 min /5 min, 5000cyc	77*3	0 Fail	Pass
15	D-HTOL	BUCK, Vin=32V, Vout=13.5V, Iout=7A, Fsw=1.2MHz, Tj=125°C, 1000hrs	8set*3	0 Fail	Pass
16	RSH	260±5℃, 10±1s	45*1	0 Fail	Pass
17	Solderability	1.Precondition Condition C (8hrs) 2.Temperature and time: Pb-free, 245±5°C, 5±0.5s	22*3	0 Fail	Pass
18	DPA	Random sample of parts that have successfully completed H3TRB or HAST, and TC	4*1	0 Fail	Pass

Note： 1. ESD-HBM/ESD-CDM/ Solderability/RSH outsource test by the third-party laboratory.
2. Others reliability implement in Innoscience (ZH)

4.1 High Temperature Reverse Bias (HTRB)

Parts were subjected to 100% of the drain-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the AEC-Q101 Standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
HTRB	INN040FQ045A-Q	Ta=150°C, VD=40V, VG=VS=0V	0	77 x 3	1000

4.2 High Temperature Gate Bias (HTGB(+))

Parts were subjected to 100% of the rated positive gate-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the AEC-Q101 Standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
HTGB(+)	INN040FQ045A-Q	Ta=150°C, VG=6V, VD=VS=0V	0	77 x 3	1000

4.3 High Temperature Gate Bias (HTGB(-))

Parts were subjected to 100% of the negative gate-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the Qual. plan.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
HTGB(-)	INN040FQ045A-Q	T=150°C, VG=-4V, VD=VS=0V	0	77 x 3	1000

4.4 Low Temperature Reverse Bias (LTRB)

Parts were subjected to 100% of the rated drain-source voltage with the ambient temperature of -40°C for a stress period of 1000 hours. The testing was done in accordance with the Qual. Plan

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
LTRB	INN040FQ045A-Q	Ta=-40°C, VD=40V, VG=VS=0V	0	77 x 3	1000

4.5 Low Temperature Gate Bias (LTGB(+))

Parts were subjected to 100% of the positive gate-source bias with the ambient temperature of -40°C for a stress period of 1000 hours. The testing was done in accordance with the Qual. plan.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
LTGB(+)	INN040FQ045A-Q	T=-40°C, VG=6V, VD=VS=0V	0	77 x 3	1000

4.6 Electro-Static discharge (ESD-HBM)

Parts were subjected to HBM (ESDA/JEDEC JS-001) test to guarantee the device can stand electrostatic voltage during handling.

Test Item	Product Number	Test Condition	Passed Voltage	Sample Size (Unit x Lot)	JEDEC Class
HBM	INN040FQ045A-Q	Ta=25°C	(±) 500V	30 x 1	Class 1B

4.7 Electro-Static discharge (ESD-CDM)

Parts were subjected to CDM (ESDA/JEDEC JS-002) test to guarantee the device can stand electrostatic voltage during handling.

Test Item	Product Number	Test Condition	Passed Voltage	Sample Size (Unit x Lot)	JEDEC Class
CDM	INN040FQ045A-Q	Ta=25°C	(±) 500V	30 x 1	Class 2a

4.8 Moisture Sensitivity Level (MSL1)

Parts were baked at 125°C for 24 hours, and then subjected to 85%RH at 85°C for a stress period of 168 hours. The parts were also subjected to three cycles of Pb-free reflow in accordance with the AEC-Q101 standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
MSL1	INN040FQ045A-Q	T=85°C, RH=85%, 3 x reflow	0	25 x 3	168

4.9 High Humidity, High Temperature Reverse Bias (H^3TRB)

Parts were subjected to 80% of the rated drain-source bias at 85%RH and 85°C for a stress period of 1000 hours. The testing was done in accordance with the AEC-Q101 Standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
H^3TRB	INN040FQ045A-Q	Ta=85°C, 85% RH, VD=32V, VG=VS=0V	0	77 x 3	1000

4.10 Temperature Cycling (TC)

Parts were subjected to temperature cycling between -55°C and +150°C for a total of 1000 cycles. Heating rate and cooling rate of 15°C /min. Dwell time of 5 minutes were used in accordance with the AEC-Q101 Standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Cys)
TC	INN040FQ045A-Q	-55°C/150°C,15°C/min, 5min dwell time	0	77 x 3	1000

4.11 TC Delamination Test (TCDT)

Random 2ea Parts were subjected to do DPA from the device after 1000Cyc. TC mentioned in 4.2. Focused on analysis the highest stress point and related gate, source, drain point. Followed the DPA standard mentioned in 4.17. The method is in accordance with the AEC-Q101 standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)
TCDT	INN040FQ045A-Q	Choose random 2parts after TC, analysis the highest stress point and related gate, source, drain point	0	2 x 3

4.12 Unbiased Highly Accelerated Temperature and Humidity Stress Test (uHAST)

Parts were subjected to 85%RH and 130°C for a stress period of 96 hours. The testing was done in accordance with the AEC-Q101 Standard.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
uHAST	INN040FQ045A-Q	Ta=130°C, 85% RH	0	77 x 3	96

4.13 Thermal Shock (TS)

Parts were subjected to temperature cycling between -55°C and +150°C for a total of 1000 cycles with 10s transfer time. Dwell time of 15 minutes were used in accordance with the Qual. Plan.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Cys)
TS	INN040FQ045A-Q	Ta=-55°C to 150°C Transfer time:10s Dwell time:15mins	0	77 x 3	1000

4.14 Intermittent Operating Life (IOL)

Parts are subjected to power cycled over ΔT=125°C temperature range. Devices are heated through internal electrical power dissipation with combined gate and drain bias, and a regulated drain current. With one minutes temperature ramp, and five minutes cool down for a stress period of 5000 cycles. The testing was done in accordance with the MIL-STD-750 (Method 1037).

Test Items	Part Number	Test Conditions	Fail #s	Sample Size (SS x Lot)	Duration
IOL	INN040FQ045A-Q	ΔTj =125°C,Tjmax=125°C Ton/Toff=1min/5min	0	77 x 3	5000Cys

4.15 Dynamic High Temperature Operating Life (D-HTOL)

Parts were subjected to DC-to-DC system test adapted BUCK topology at Tj=125°C for a stress period of 1000 hours. The testing was done in accordance with the JEDEC standard JEP-180.

Test Item	Product Number	Test Condition	Fail #	Sample Size (Set x Lot)	Duration (Hrs)
D-HTOL	INN040FQ045A-Q	BUCK, Vin=32V, Vout=13.5V, Iout=7A, Fsw=1.2MHz, Tj=125°C, 1000hrs	0	8set x 3	1000

4.16 Resistance to Solder Heat (RSH)

Parts were subjected to solder immersion condition after bake, soak. The testing was done in accordance with the AEC-Q101 Standard.

Test Item	Product Number	Test Condition	Sample Size (Unit x Lot)	Fail criteria
RSH	INN040FQ045A-Q	260±5°C, 10±1s	45 x 1	0 Fail

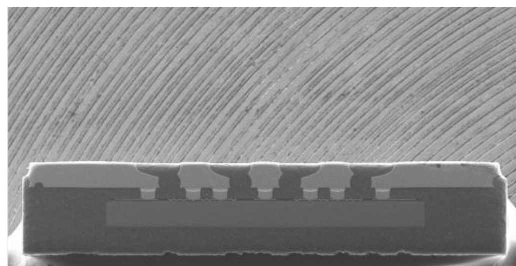
4.17 Solderability

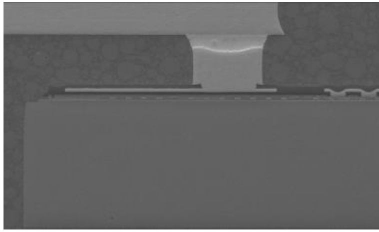
Parts were subjected to surface mount process then reflow test. The testing was done in accordance with the AEC-Q101 Standard.

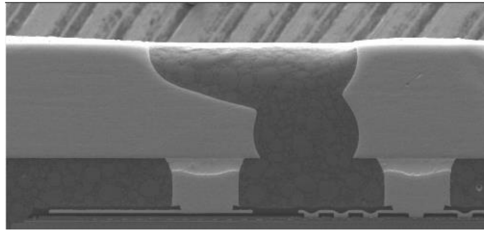
Test Item	Product Number	Test Condition	Sample Size (Unit x Lot)	Fail criteria
Solderability	INN040FQ045A-Q	1.Precondition Condition C (8hrs) 2.Temperature and time: Pb-free, 245±5°C, 5±0.5s	22 x 3	0 Fail

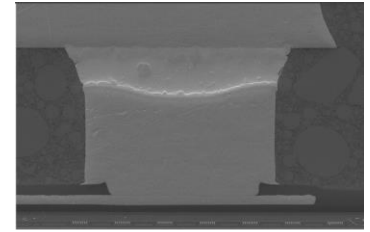
4.18 Destructive Physical Analysis (DPA)

Parts were subjected to be unsealed and to see corrosion, contamination, delamination and metal hole and the crack or defect between device and substrate, which have successfully completed H^3TRB or HAST, and TC. The method is in accordance with the AEC-Q101-004 section 4 standard.









Parts were mounted on to FR4 adaptor cards. Adaptor cards with two copper layers were used. The copper layer thickness was between 2 oz. SAC305 solder was used to mount the DUTs onto the adaptor cards.

Revision/Updated History

Revision	Reason for Change	Date	Prepared by	Approved by
V1.0	Initial release	Jun./28/2024	Huahui Wang Jieming Yin	RE center: Blanck, Director
V1.1	Idss re-spec	July/11/2024	Huahui Wang Jieming Yin	RE center: Jianping Wang, VP